中关村芯园EDA平台Cadence常用工具

Product ID	Product Description	Product Sector	External Family
111	Cadence(R) Design Framework II	Custom Environment & Layout	Virtuoso Layout Suite
117	Cadence Framework Integration Runtime Option	Custom Environment & Layout	Virtuoso Schematic Editor
12141	Cadence(R) Design Framework Integrator's Toolkit	Custom Environment & Layout	Virtuoso Layout Suite
206	Virtuoso(R) Simulation Environment	Custom Environment & Layout	Virtuoso Schematic Editor
21060	Virtuoso(R) Schematic VHDL Interface	Custom Environment & Layout	Virtuoso Schematic Editor
21400	Virtuoso(R) Schematic Editor Verilog(R) Interface	Custom Environment & Layout	Virtuoso Schematic Editor
23560	Incisive Formal Verifier	Functional Verification	Incisive Formal
25010	Cadence(R) Simulation Analysis Environment (SimVision)	Functional Verification	Incisive Interactive
26000	Verilog(R)-XL Simulator	Functional Verification	Incisive Simulation
26262	Incisive Functional Safety Simulator	Functional Verification	Incisive Interactive
26500	Verifault(R)-XL simulator	Functional Verification	Incisive Interactive
26510	Verifault-XL(R) Slave Node License	Functional Verification	Incisive Interactive
276	Virtuoso(R) Schematic Editor HSPICE Interface	Custom Environment & Layout	Virtuoso Schematic Editor
28020	Cadence Advanced Encryption Standard-64bit	Functional Verification	Incisive Simulation
29610	Incisive Enterprise Simulator -L	Functional Verification	Incisive Simulation
29651	Incisive Enterprise Simulator -XL	Functional Verification	Incisive Simulation
29661	Enterprise Simulator -XL Interface for MTI	Functional Verification	Incisive Simulation
29671	Enterprise Simulator -XL Interface for VCS	Functional Verification	Incisive Simulation
29710	Digital Mixed Signal Option to IES	Functional Verification	Incisive Simulation
29851	Incisive Advanced Option	Functional Verification	Incisive Simulation
29852	Incisive Debug Analyzer Option	Functional Verification	Incisive Interactive
29853	Indago Debug Analyzer App	Functional Verification	Incisive Interactive
29861	Incisive Low-Power Simulation Option	Functional Verification	Incisive Simulation
29862	Indago Embedded Software Debug App	Functional Verification	Incisive Interactive
29875	Incisive Advanced HAL Option	Functional Verification	Incisive Interactive
29SDPAPXP	Option: Palladium XP Dynamic Power Analysis	Emulation & Acceleration	Palladium XP
3002	Virtuoso Digital Implementation	Digital Implementation	Encounter VDI
3003	Virtuoso Digital Implementation XL	Digital Implementation	Encounter VDI
3004	VDI-XL Block Capacity Option	Digital Implementation	Encounter VDI
32100	Virtuoso(R) Analog Oasis Run-Time Option	Custom Environment & Layout	Virtuoso Legacy -Environment
32101	Cadence(R) OASIS for RFDE	Custom Environment & Layout	Virtuoso Legacy -Environment
32501	Virtuoso(R) Spectre Model Interface Option	Circuit Simulation & Characterizatio	Spectre
32760	Virtuoso(R) Analog HSPICE Interface Option	Custom Environment & Layout	Virtuoso Legacy -Environment
33400	Virtuoso UltraSim Simulator	Circuit Simulation & Characterizatio	UltraSim
33580	Virtuoso(R) RelXpert	Circuit Simulation & Characterizatio	UltraSim
3500	Spectre Characterization Simulator Option	Circuit Simulation & Characterizatio	Spectre
365	Dracula(R) Graphical User Interface	Physical Signoff	Signoff DRC/LVS
38500	Spectre(R) Classic Simulator	Circuit Simulation & Characterizatio	Spectre
38510	Virtuoso Advanced Simulation Interface Option to Virtuoso Spectre Simulator -L	Circuit Simulation & Characterizatio	Spectre
38520	Spectre(R) -RF option for 38500 and 91050	Circuit Simulation & Characterizatio	Spectre RF
39HAHWD	Palladium XP XL license on-demand, one additional domain capacity up to the physical limit of the system option	Emulation & Acceleration	Palladium XP
39HLHWD	Palladium XP II XL License on-demand	Emulation & Acceleration	Palladium XP II
39HPHWD	Palladium XP GXL license on-demand, one additional domain capacity up to the physical limit of the system option	Emulation & Acceleration	Palladium XP

中关村芯园（北京）有限公司 地址：北京市海淀区中关村创业大街4号楼4层 邮编：100080 Tel：(010) 82484010/4090/4510/4520转828 Fax：4008266163-26880 Web：www.zgcicc.com

39HUMEM	Option: Palladium Series Memory-model Single Subscription	Emulation & Acceleration	Palladium XP
39HUMEMM	Option: Palladium Series Memory-model Multiple Subscription	Emulation & Acceleration	Palladium XP
39HUVJTAG4	Virtual JTAG Debug Interface to Lauterbach Trace32 4-pack	Emulation & Acceleration	Palladium XP
39HXHWD	Palladium XP II GXL license on-demand	Emulation & Acceleration	Palladium XP II
39R2001	Protium Implementation and Debug Software	Emulation & Acceleration	Rapid Prototyping
70000	Virtuoso(R) AMS Designer Environment	Custom Environment & Layout	Virtuoso AMS Environment
70020	AMS Designer with Flexible Analog Simulation	Circuit Simulation & Characterizatio	AMS Designer
70030	Virtuoso AMS Designer Verification Option	Circuit Simulation & Characterizatio	AMS Designer
70110	Dracula(R) Design Rule Checker	Physical Signoff	Signoff DRC/LVS
70120	Dracula(R) Layout Vs. Schematic Verifier	Physical Signoff	Signoff DRC/LVS
70130	Dracula(R) Parasitic Extractor	Physical Signoff	Signoff DRC/LVS
70510	Dracula(R) Physical Verification Suite	Physical Signoff	Signoff DRC/LVS
70520	Dracula(R) Physical Verification and Extraction Suite	Physical Signoff	Signoff DRC/LVS
71110	Diva(R) Design Rule Checker	Physical Signoff	Signoff DRC/LVS
71120	Diva(R) Layout Vs. Schematic Verifier	Physical Signoff	Signoff DRC/LVS
71130	Diva(R) Parasitic Extractor	Physical Signoff	Signoff DRC/LVS
71510	Diva(R) Physical Verification Suite	Physical Signoff	Signoff DRC/LVS
71520	Diva(R) Physical Verification and Extraction Suite	Physical Signoff	Signoff DRC/LVS
72110	Assura(TM) Design Rule Checker	Physical Signoff	Signoff DRC/LVS
72120	Assura(TM) Layout Vs. Schematic Verifier	Physical Signoff	Signoff DRC/LVS
72140	Assura(TM) Graphical User Interface Option	Physical Signoff	Signoff DRC/LVS
72150	Assura(TM) Multiprocessor Option	Physical Signoff	Signoff DRC/LVS
74020	Cadence Yield Analyzer and Optimizer	Physical Signoff	Signoff DFM
900	Cadence(R) SKILL Development Environment	Custom Environment & Layout	Virtuoso Layout Suite
90004	Spectre Multi-mode Simulation	Circuit Simulation & Characterizatio	MMSim
91050	Spectre(R) Accelerated Parallel Simulator	Circuit Simulation & Characterizatio	Spectre
91400	Spectre(R) Power Option	Circuit Simulation & Characterizatio	MMSim
91500	Spectre(R) CPU Accelerator Option	Circuit Simulation & Characterizatio	MMSim
91700	Spectre Electromigration and IR Drop Simulator 3 pack	Circuit Simulation & Characterizatio	Spectre
940	Virtuoso(R) EDIF 200 Reader	Custom Environment & Layout	Virtuoso Layout Suite
945	Virtuoso(R) EDIF 200 Writer	Custom Environment & Layout	Virtuoso Layout Suite
95100	Virtuoso(R) Schematic Editor L	Custom Environment & Layout	Virtuoso Schematic Editor
95115	Virtuoso(R) Schematic Editor XL	Custom Environment & Layout	Virtuoso Schematic Editor
95200	Virtuoso(R) Analog Design Environment L	Custom Environment & Layout	Virtuoso Analog Design Environment
95210	Virtuoso(R) Analog Design Environment XL	Custom Environment & Layout	Virtuoso Analog Design Environment
95220	Virtuoso(R) Analog Design Environment -GXL	Custom Environment & Layout	Virtuoso Analog Design Environment
95222	Token Control for Virtuoso(R) Analog Design Environment -GXL	Custom Environment & Layout	Virtuoso Analog Design Environment
95230	Virtuoso LDE Analyzer Option	Custom Environment & Layout	Virtuoso Layout Suite
95250	Virtuoso(R) ADE Explorer	Custom Environment & Layout	Virtuoso Analog Design Environment
95255	Virtuoso(R) Visualization & Analysis XL	Custom Environment & Layout	Virtuoso Analog Design Environment
95260	Virtuoso(R) ADE Assembler	Custom Environment & Layout	Virtuoso Analog Design Environment
95265	Virtuoso(R) Variation Option	Custom Environment & Layout	Virtuoso Analog Design Environment
95270	Virtuoso(R) ADE Verifier	Custom Environment & Layout	Virtuoso Analog Design Environment
95300	Virtuoso(R) Layout Suite L	Custom Environment & Layout	Virtuoso Layout Suite
95310	Virtuoso(R) Layout Suite XL	Custom Environment & Layout	Virtuoso Layout Suite

95311	Virtuoso(R) DFM Option	Custom Environment & Layout	Virtuoso Layout Suite
95321	Virtuoso(R) Layout Suite -GXL	Custom Environment & Layout	Virtuoso Layout Suite
95322	Token Control for Virtuoso(R) Layout Suite -GXL	Custom Environment & Layout	Virtuoso Layout Suite
95323	Virtuoso Layout Suite GXL	Custom Environment & Layout	Virtuoso Layout Suite
95324	Token Control for Virtuoso Layout Suite GXL	Custom Environment & Layout	Virtuoso Layout Suite
95512	Virtuoso Advanced Node Option for Layout Standard	Custom Environment & Layout	Virtuoso Layout Suite
95600	Virtuoso Layout Suite EAD	Custom Environment & Layout	Virtuoso Layout Suite
95610	Virtuoso EAD 3D Precision Solver	Custom Environment & Layout	Virtuoso Layout Suite
95620	Virtuoso EAD Advanced Electrical Analysis	Custom Environment & Layout	Virtuoso Layout Suite
95710	Virtuoso Mixed Signal Option for Layout	Custom Environment & Layout	Virtuoso Layout Suite
96210	Cadence(R) Physical Verification System Design Rule Checker XL	Physical Signoff	Signoff DRC/LVS
96220	Cadence(R) Physical Verification System Layout vs. Schematic Checker XL	Physical Signoff	Signoff DRC/LVS
96230	Cadence(R) Physical Verification System Programmable Electrical Rules Checker	Physical Signoff	Signoff DRC/LVS
96235	Cadence Physical Verification System Programmable Electrical Rules Checker XL	Physical Signoff	Signoff DRC/LVS
96240	Cadence(R) Physical Verification System Results Manager	Physical Signoff	Signoff DRC/LVS
96245	Cadence(R) Physical Verification System Design Analysis Option	Physical Signoff	Signoff DRC/LVS
96246	Cadence Physical Verification System QuickView Signoff Environment	Physical Signoff	Signoff DRC/LVS
96300	Cadence(R) Physical Verification System Constraint Validator	Physical Signoff	Signoff DRC/LVS
96305	Cadence Physical Verification System Constraint Validator XL	Physical Signoff	Signoff DRC/LVS
96330	Cadence(R) Physical Verification System Advanced Device Option	Physical Signoff	Signoff DRC/LVS
96340	Cadence(R) Physical Verification System Pattern Matching Option	Physical Signoff	Signoff DRC/LVS
96350	Cadence(R) Physical Verification System Mask Rule Check Option	Physical Signoff	Signoff DRC/LVS
96400	Virtuoso(R) Integrated Physical Verification System Option for Virtuoso Layout Suite (95300, 95310)	Physical Signoff	Signoff DRC/LVS
ALT110	Virtuoso Liberate Server	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT111	Virtuoso Liberate Client	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT210	Virtuoso Variety Server	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT211	Virtuoso Variety Client	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT310	Package of Virtuoso Liberate and Variety Server	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT311	Package of Virtuoso Liberate and Variety Client	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT410	Virtuoso Liberate MX Server	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT411	Virtuoso Liberate MX Client	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT610	Virtuoso Liberate LV Server	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT611	Virtuoso Liberate LV Client	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT710	Package of Virtuoso Liberate and Liberate LV Server	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT711	Package of Virtuoso Liberate and Liberate LV Client	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT810	Virtuoso Liberate AMS Server	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT811	Virtuoso Liberate AMS Client with Spectre/APS for Characterization	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
ALT812	Virtuoso Liberate AMS Client	Circuit Simulation & Characterizatio	Virtuoso Foundation IP Characterization
CFM100	Conformal -L (a.k.a Conformal ASIC)	Formal Verification	Conformal Equivalency Checker
CFM200	Conformal -XL (a.k.a Conformal Ultra)	Formal Verification	Conformal Equivalency Checker
CFM300	Conformal -GXL (a.k.a Conformal Custom)	Formal Verification	Conformal Equivalency Checker
CFM401	Conformal Constraint Designer -L	Formal Verification	Conformal Constraint Designer
CFM421	Conformal Constraint Designer -XL	Formal Verification	Conformal Constraint Designer
CFM422	CCD Multi-Constraint Check Option	Formal Verification	Conformal Constraint Designer
CFM500	Conformal Low Power -XL	Formal Verification	Conformal Low Power

CFM550	Conformal Low Power -GXL	Formal Verification	Conformal Low Power
CMP205	Cadence CMP Predictor Basic -FEOL	Physical Signoff	Signoff DFM
CMP206	Cadence CMP Predictor -FEOL	Physical Signoff	Signoff DFM
CMP208	Cadence CMP Process Optimizer with Predictor and Calibrator 鈥?FEOL	Physical Signoff	Signoff DFM
CMP209	Cadence CMP Predictor -8 CPU Distributed Processing Pack	Physical Signoff	Signoff DFM
CMP305	Cadence CMP Predictor - Basic -BEOL and MOL	Physical Signoff	Signoff DFM
CMP306	Cadence CMP Predictor - BEOL and MOL	Physical Signoff	Signoff DFM
CMP308	Cadence CMP Process Optimizer with Predictor and Calibrator -BEOL and MOL	Physical Signoff	Signoff DFM
EDS03	Encounter CPU Accelerator Option	Digital Implementation	Encounter Advanced Options
EDS10	Encounter Low Power GXL Option	Digital Implementation	Encounter Advanced Options
EDS100	Encounter Digital Implementation System L	Digital Implementation	Encounter Base
EDS20	Encounter Mixed Signal GXL Option	Digital Implementation	Encounter Advanced Options
EDS200	Encounter Digital Implementation System XL	Digital Implementation	Encounter Base
EDS210	Encounter Clock Concurrent Optimization	Digital Implementation	Encounter CCOpt
EDS30	Encounter Advanced Node GXL Option	Digital Implementation	Encounter Advanced Options
EDS300	EDI System Block Design	Digital Implementation	Encounter Base
EDS310	EDI System Hierarchical Design Option	Digital Implementation	Encounter Hierarchical
EDS50	Encounter DFM GXL Option	Digital Implementation	Encounter Advanced Options
EDS60	Encounter Stacked Die GXL Option	Digital Implementation	Encounter 3DIC
EDS70	Encounter Giga Scale GXL Option	Digital Implementation	Encounter Advanced Options
EDSI20	Encounter I20 GXL Option	Digital Implementation	Encounter Advanced Options
EDSS20	Encounter S20 GXL Option	Digital Implementation	Encounter Advanced Options
EDST20	Encounter T20 GXL Option	Digital Implementation	Encounter Advanced Options
EDSU20	Encounter Universal 20 GXL Option	Digital Implementation	Encounter Advanced Options
ET008	Encounter Diagnostics Yield Environment -XL	Synthesis & Test	Encounter Diagnostics
ET010	Encounter Diagnostics Basic	Synthesis & Test	Encounter Diagnostics
ET020	Option to RC -DFT Architect Basic	Synthesis & Test	Encounter DFT Architect
ET021	Option to RC -DFT Architect Advanced	Synthesis & Test	Encounter DFT Architect
ET022	Encounter True Time ATPG Basic	Synthesis & Test	Encounter True-Time ATPG
ET023	Encounter True Time ATPG Advanced	Synthesis & Test	Encounter True-Time ATPG
ET024	Encounter Test Advanced MBIST Option	Synthesis & Test	Encounter DFT Architect
ET025	Encounter Test LBIST Option	Synthesis & Test	Encounter DFT Architect
ET026	Encounter Test Hierarchical Option	Synthesis & Test	Encounter DFT Architect
FE100GPS	First Encounter -XL (aka Cadence (R) First Encounter -GPS)	Digital Implementation	Encounter First Encounter
FE80	First Encounter -L (aka First Encounter VIP)	Digital Implementation	Encounter First Encounter
GEN100	Genus Synthesis Solution	Synthesis & Test	Genus
GEN30	Genus Low Power Option	Synthesis & Test	Genus
GEN40	Genus Physical Option	Synthesis & Test	Genus Physical
GEN80	Genus CPU Accelerator Option	Synthesis & Test	Genus
IEV101	Incisive Enterprise Verifier -XL	Functional Verification	Incisive Formal
IEV102	Incisive Coverage Unreachability App	Functional Verification	Incisive Formal
INT107	PPC Interactive Optimizer Turbo	Physical Signoff	Signoff Manufacturing
INVS10	Innovus 10nm Option	Digital Implementation	Innovus
INVS100	Innovus Implementation System	Digital Implementation	Innovus
INVS20	Innovus 20/16/14nm Option	Digital Implementation	Innovus

INVS30	Innovus Mixed Signal Option	Digital Implementation	Innovus
INVS40	Innovus Hierarchical Design Option	Digital Implementation	Innovus
INVS50	Innovus DFM Option	Digital Implementation	Innovus
INVS60	Innovus 3D-IC Option	Digital Implementation	Innovus
INVS80	Innovus CPU Accelerator Option	Digital Implementation	Innovus
INVS95	Innovus Implementation System -Basic	Digital Implementation	Innovus
INVSI10	Innovus 110nm Option	Digital Implementation	Innovus
INVSI20	Innovus 120nm Option	Digital Implementation	Innovus
JGAFL100	JasperGold Automatic Formal Linting App	Functional Verification	Jasper Formal
JGCON100	JasperGold Connectivity Verification APP	Functional Verification	Jasper Formal
JGCONOPT	JasperGold Connectivity Verification APP Option to 23560 or IEV101	Functional Verification	Jasper Formal
JGCOV100	JasperGold Coverage APP Option	Functional Verification	Jasper Formal
JGCSR100	JasperGold CSR Verification APP	Functional Verification	Jasper Formal
JGCSROPT	JasperGold CSR Verification APP Option to 23560 or IEV101	Functional Verification	Jasper Formal
JGFPV100	JasperGold Formal Property Verification APP	Functional Verification	Jasper Formal
JGFPVOPT	JasperGold Formal Property Verification APP Option to 23560 or IEV101	Functional Verification	Jasper Formal
JGINT100	JasperGold Interactive Option	Functional Verification	Jasper Formal
JGLPV100	JasperGold Low Power Verification APP	Functional Verification	Jasper Formal
JGSEC100	JasperGold Sequential Equivalency Checking APP	Functional Verification	Jasper Formal
JGSPSOPT	JasperGold Structural Property Synthesis APP Option to 23560 or IEV101	Functional Verification	Jasper Formal
JGXPR100	JasperGold X-Propagation Verification APP	Functional Verification	Jasper Formal
JGXPROPT	JasperGold X-Propagation Verification APP Option to 23560 or IEV101	Functional Verification	Jasper Formal
JLS100	Joules RTL Power Solution	Synthesis & Test	Joules
K2110	MaskCompose Definition Module	Physical Signoff	Signoff DRC/LVS
K2120	MaskCompose Implementation Module	Physical Signoff	Signoff DRC/LVS
K2122	MaskCompose OASIS Option	Physical Signoff	Signoff DRC/LVS
K2130	MaskCompose Paperwork Module	Physical Signoff	Signoff DRC/LVS
K2140	MaskCompose Fracture Prep/Jobdeck Module	Physical Signoff	Signoff DRC/LVS
K2142	MaskCompose SemiP10 Option	Physical Signoff	Signoff DRC/LVS
K2150	MaskCompose Wafer Module	Physical Signoff	Signoff DRC/LVS
K2200	Cadence(R) QuickView Layout and Mask Data Viewer	Physical Signoff	Signoff DRC/LVS
K2210	Cadence(R) QuickView Layout Data Viewer	Physical Signoff	Signoff DRC/LVS
K2211	Cadence QuickView Sign-Off Data Analysis Environment	Physical Signoff	Signoff DRC/LVS
K2220	Cadence(R) QuickView Mask Data Viewer	Physical Signoff	Signoff DRC/LVS
K2302	Chameleon Basic	Physical Signoff	Signoff DRC/LVS
K2330	Chameleon LV Slave	Physical Signoff	Signoff DRC/LVS
K2335	Chameleon PG Slave	Physical Signoff	Signoff DRC/LVS
K2345	Chameleon PG Option	Physical Signoff	Signoff DRC/LVS
LPA102	Cadence Litho Physical Analyzer Basic	Physical Signoff	Signoff DFM
LPA120	Cadence Litho Hotspot Fixing Option	Physical Signoff	Signoff DFM
P6191	Virtuoso Advanced Device Modeling HVMOS (For Eldo)	Circuit Simulation & Characterizatio	Device Modeling
P6192	Virtuoso Advanced Device Modeling HVMOS (For HSPICE)	Circuit Simulation & Characterizatio	Device Modeling
PA1410	Allegro Design Authoring High-Speed Option	PCB Design	PCB Design -Front End
PA1510	Allegro Design Authoring Multi-Style Option	PCB Design	PCB Design -Front End
PA1720	Allegro(R) Design Authoring Team Design Option	PCB Design	PCB Design -Front End

PA3100	Allegro PCB Designer	PCB Design	PCB Design -Layout
PA3110	Allegro PCB High-Speed Option	PCB Design	PCB Design -Layout
PA3120	Allegro PCB Miniaturization Option	PCB Design	PCB Design -Layout
PA3130	Allegro PCB Manufacturing Option	PCB Design	PCB Design -Layout
PA3150	Allegro PCB Productivity Toolbox Option	PCB Design	PCB Design -Layout
PA3200	Allegro Relational Rules Developer	PCB Design	PCB Design -Layout
PA3210	Allegro Relational Rules Checker	PCB Design	PCB Design -Layout
PA3410	Allegro(R) PCB Team Design Option	PCB Design	PCB Design -Layout
PA3420	Allegro(R) PCB Analog/RF Option	PCB Design	PCB Design -Layout
PA3670	Allegro PCB Design Planning Option	PCB Design	PCB Design -Layout
PA5700	Allegro Sigrity SI Base	PCB Design	Power and Signal Integrity Analysis
PA5750	Allegro Sigrity High-Speed Base	PCB Design	Power and Signal Integrity Analysis
PA5800	Allegro Sigrity PI Base	PCB Design	Power and Signal Integrity Analysis
PA6605	Cadence 3D Design Viewer	IC Package/SiP co-design	IC Packaging/SiP co-design
PA8250	Allegro 2 FPGA System Planner Option	PCB Design	PCB Design -Front End
PA8610	Allegro(R) 4 FPGA System Planner Option	PCB Design	PCB Design -Front End
PA8630	Allegro(R) ASIC Prototyping with FPGA's	PCB Design	PCB Design -Front End
PASASG	Generator to generate Assura compatible verification decks	Custom Environment & Layout	PDK Automation System
PASCAG	Generator to generate Calibre(TM) compatible verification decks	Custom Environment & Layout	PDK Automation System
PASDIG	Generator to generate Diva compatible verification decks	Custom Environment & Layout	PDK Automation System
PASECG	Error Cell Generator	Custom Environment & Layout	PDK Automation System
PASGTE	Graphical Technology Editor	Custom Environment & Layout	PDK Automation System
PASPCG	Pcell Generator	Custom Environment & Layout	PDK Automation System
PDW123	Allegro Design Workbench PDM Option	PCB Design	PCB Design -Front End
PDW503	Allegro(R) Design Workbench	PCB Design	PCB Design -Front End
PDW623	Allegro(R) Library Workbench	PCB Design	PCB Design -Front End
PDW703	Allegro(R) Library Server	PCB Design	PCB Design -Front End
PPC100	PPC Model Builder	Physical Signoff	Signoff Manufacturing
PPC101	PPC Workbench	Physical Signoff	Signoff Manufacturing
PPC102	PPC Flow Manager	Physical Signoff	Signoff Manufacturing
PPC103	PPC Distributed Processing	Physical Signoff	Signoff Manufacturing
PPC104	PPC Interactive Optimizer	Physical Signoff	Signoff Manufacturing
PPC110	Contour Option to PPC Model Builder	Physical Signoff	Signoff Manufacturing
PPC111	Verification Option to PPC Workbench	Physical Signoff	Signoff Manufacturing
PPC112	MB-SRAF Manager	Physical Signoff	Signoff Manufacturing
PPC113	MB-SRAF Distribution	Physical Signoff	Signoff Manufacturing
PPC114	PPC Model DP	Physical Signoff	Signoff Manufacturing
PPC200	Cadence PPC Distributed Processing (200 CPU Pack)	Physical Signoff	Signoff Manufacturing
PPC203	Cadence PPC Distributed Processing (4 CPU Pack)	Physical Signoff	Signoff Manufacturing
PPC204	Cadence PPC Distributed Processing Option to PPC200 (25 CPU Pack)	Physical Signoff	Signoff Manufacturing
PPC212	Cadence PPC RB-SRAF Manager	Physical Signoff	Signoff Manufacturing
PPC213	Cadence PPC Hybrid SRAF optimization	Physical Signoff	Signoff Manufacturing
PPC220	Cadence PPC Pattern Analysis Option	Physical Signoff	Signoff Manufacturing
PPC230	Cadence PPC Multi-Patterning Option	Physical Signoff	Signoff Manufacturing
PPC301	Cadence PPC Workbench (5 Pack)	Physical Signoff	Signoff Manufacturing

PPC302	Cadence PPC Flow Manager (5 Pack)	Physical Signoff	Signoff Manufacturing
PPC312	Cadence PPC RB-SRAF Manager (5 Pack)	Physical Signoff	Signoff Manufacturing
PPC313	Cadence PPC Hybrid SRAF Optimization (5 Pack)	Physical Signoff	Signoff Manufacturing
PS2000	Allegro(R) Design Authoring	PCB Design	PCB Design -Front End
PS2005	Allegro Design Entry Capture	PCB Design	PCB Design -Front End
PS2010	Allegro(R) Design Entry CIS	PCB Design	PCB Design -Front End
PS2200	Allegro(R) AMS Simulator	PCB Design	PCB Design -Front End
PS3500	Allegro PCB Routing Option	PCB Design	PCB Design -Layout
PX3500	Allegro(R) PCB Librarian	PCB Design	PCB Design -Front End
PX3600	Allegro(R) Physical Viewer	PCB Design	PCB Design -Layout
PX4100	Allegro(R) Package Designer -L	IC Package/SiP co-design	IC Packaging/SiP co-design
QRCX100	Cadence Quantus QRC Extraction -L	Electrical Signoff	Signoff Extraction
QRCX300	Cadence Quantus QRC Extraction -XL	Electrical Signoff	Signoff Extraction
QRCX310	Cadence Quantus QRC Advanced Analysis GXL Option	Electrical Signoff	Signoff Extraction
QRCX320	Cadence Quantus QRC Advanced Modeling GXL Option	Electrical Signoff	Signoff Extraction
QRCX330	Cadence Quantus QRC Display Technology Option	Electrical Signoff	Signoff Extraction
QRCX530	Cadence Quantus QRC Advanced Node Modeling Option	Electrical Signoff	Signoff Extraction
SIGR004	Sigrity Parallel Computing 4 Pack	PCB Design	Power and Signal Integrity Analysis
SIGR011	Broadband SPICE	PCB Design	Power and Signal Integrity Analysis
SIGR021	Transistor to Behavioral Model Conversion	PCB Design	Power and Signal Integrity Analysis
SIGR031	CAD Design/Data Translators	PCB Design	Power and Signal Integrity Analysis
SIGR051	OptimizePI	PCB Design	Power and Signal Integrity Analysis
SIGR106	OrbitIO	IC Package/SiP co-design	IC Packaging/SiP co-design
SIGR201	PowerDC	PCB Design	Power and Signal Integrity Analysis
SIGR301	PowerSI	PCB Design	Power and Signal Integrity Analysis
SIGR311	PowerSI 3D EM Full-Wave Extraction Option	PCB Design	Power and Signal Integrity Analysis
SIGR401	SPEED2000	PCB Design	Power and Signal Integrity Analysis
SIGR506	SystemSI -Serial Link Analysis II	PCB Design	Power and Signal Integrity Analysis
SIGR556	SystemSI -Parallel Bus Analysis II	PCB Design	Power and Signal Integrity Analysis
SIGR570	Sigrity System Explorer	PCB Design	Power and Signal Integrity Analysis
SIGR575	Sigrity SystemSI Suite	PCB Design	Power and Signal Integrity Analysis
SIGR625	Advanced Package Router Option	IC Package/SiP co-design	IC Packaging/SiP co-design
SIGR706	XcitePI Simulation	PCB Design	Power and Signal Integrity Analysis
SIGR726	XcitePI Extraction	PCB Design	Power and Signal Integrity Analysis
SIGR801	XtractIM	PCB Design	Power and Signal Integrity Analysis
SIGR915	Allegro Sigrity Power Aware SI Option	PCB Design	Power and Signal Integrity Analysis
SIGR925	Allegro Sigrity Power Integrity Signoff and Optimization Option	PCB Design	Power and Signal Integrity Analysis
SIGR935	Allegro Sigrity System Serial Link Option	PCB Design	Power and Signal Integrity Analysis
SIGR945	Allegro Sigrity Package Assessment and Extraction Option	PCB Design	Power and Signal Integrity Analysis
SIGR950	Cadence IO-SSO Analysis Suite	PCB Design	Power and Signal Integrity Analysis
SIGR955	Voltus IC Power Integrity Solution -Sigrity Package Analysis (VTS-SPA) (Package Analysis Option to Voltus-AA)	PCB Design	Power and Signal Integrity Analysis
SIGR960	Sigrity PKG-PCB PI Voltus Suite	PCB Design	Power and Signal Integrity Analysis
SIGR965	Sigrity PKG-PCB SSO Voltus Suite	PCB Design	Power and Signal Integrity Analysis
SIP110	Cadence SiP Digital Architect -XL	IC Package/SiP co-design	IC Packaging/SiP co-design
SIP225	Cadence SiP Layout -XL	IC Package/SiP co-design	IC Packaging/SiP co-design

SL26262	Incisive Functional Safety Simulator	Functional Verification	Incisive Interactive
SMN100	Incisive Enterprise Specman Elite Testbench	Functional Verification	Incisive Simulation
SPT256U	Allegro(R) PCB Router 256U	PCB Design	PCB Design -Layout
SPT6U	Allegro(R) PCB Router 6U	PCB Design	PCB Design -Layout
SPTADV	Allegro(R) PCB Router ADV	PCB Design	PCB Design -Layout
SPTDFM	Allegro(R) PCB Router DFM	PCB Design	PCB Design -Layout
SPTHP	Allegro(R) PCB Router HP	PCB Design	PCB Design -Layout
STEP100	Cadence System for Testing PDKs FE	Custom Environment & Layout	PDK Automation System
STEP110	Cadence System for Testing PDKs Pcell	Custom Environment & Layout	PDK Automation System
STEP120	Cadence System for Testing PDKs DRC	Custom Environment & Layout	PDK Automation System
STEP130	Cadence System for Testing PDKs LVS	Custom Environment & Layout	PDK Automation System
STR100	Stratus HLS -L	System-Level Design	High Level Synthesis
STR101	Stratus HLS -XL	System-Level Design	High Level Synthesis
STR102	Stratus IDE	System-Level Design	High Level Synthesis
STR200	Stratus Floating Point	System-Level Design	High Level Synthesis
TPS100	Tempus Timing Signoff Solution L	Electrical Signoff	Signoff Timing Analysis
TPS200	Tempus Timing Signoff Solution XL	Electrical Signoff	Signoff Timing Analysis
TPS300	Tempus Timing Signoff Solution TSO	Electrical Signoff	Signoff Timing Analysis
TPS400	Tempus Timing Signoff Solution MP	Electrical Signoff	Signoff Timing Analysis
VDS100	Virtuoso Digital Signoff Timing Solution	Electrical Signoff	Signoff Timing Analysis
VDS200	Virtuoso Digital Signoff Power Solution	Electrical Signoff	Signoff Power Analysis
VMG001	vManager Linux Client (Quantity 1)	Functional Verification	Incisive Interactive
VMG005	vManager Linux Client (Quantity 5)	Functional Verification	Incisive Interactive
VMG100	vManager Project Server	Functional Verification	Incisive Interactive
VMG200	vManager Integration Server	Functional Verification	Incisive Interactive
VMGA01	vManager Multi-Project Application	Functional Verification	Incisive Interactive
VPS100	Virtuoso(R) Power System L	Electrical Signoff	Signoff Power Analysis
VRF100	PPC Verification Manager	Physical Signoff	Signoff Manufacturing
VRF101	PPC Verification Distribution	Physical Signoff	Signoff Manufacturing
VTS100	Voltus IC Power Integrity Solution -L (VTS-L)	Electrical Signoff	Signoff Power Analysis
VTS200	Voltus IC Power Integrity Solution -XL (VTS-XL)	Electrical Signoff	Signoff Power Analysis
VTS201	Voltus IC Power Integrity Solution Advanced Analysis GXL Option (VTS-AA)	Electrical Signoff	Signoff Power Analysis
VTS300	Voltus IC Power Integrity Solution - MP (VTS-MP) (Acceleration Option to Voltus IC XL (VTS200))	Electrical Signoff	Signoff Power Analysis
VTS500	Voltus-Fi Custom Power Integrity Solution -XL	Electrical Signoff	Signoff Power Analysis